Exhibit 4

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK, INC. and MEDIATEK USA, INC.,
Petitioner,

v.

REDSTONE LOGICS LLC,
Patent Owner.

Case IPR2025-00085
Patent 8,549,339

PATENT OWNER'S PRELIMINARY RESPONSE

> wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and
>
> an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.
>
> Ex. 1001 at claim 1.

All other challenged dependent claims 2-6, 8-11, and 14 depend from claim 1 and claim 21 reads similarly to claim 1.

III. Level of Ordinary Skill in the Art

The Petition proposes that a person of ordinary skill in the art in the field of the '339 Patent "would have had at least a bachelor's degree in electrical engineering, computer engineering, computer science, or a similar field, and at least two years of industry or academic experience designing or analyzing electronic circuits, semiconductors, processors, or power management, and related firmware and software, or the equivalent." Paper 1 at 6–7. For purposes of this preliminary response, Patent Owner does not challenge that definition.

IV. Claim Construction

The Petition states "the claim terms in the '339 Patent are accorded their ordinary and customary meaning that they would have to a person having ordinary

skill in the art at the time of the alleged invention." Paper 1 at 6. For purposes of this preliminary response, Patent Owner agrees.

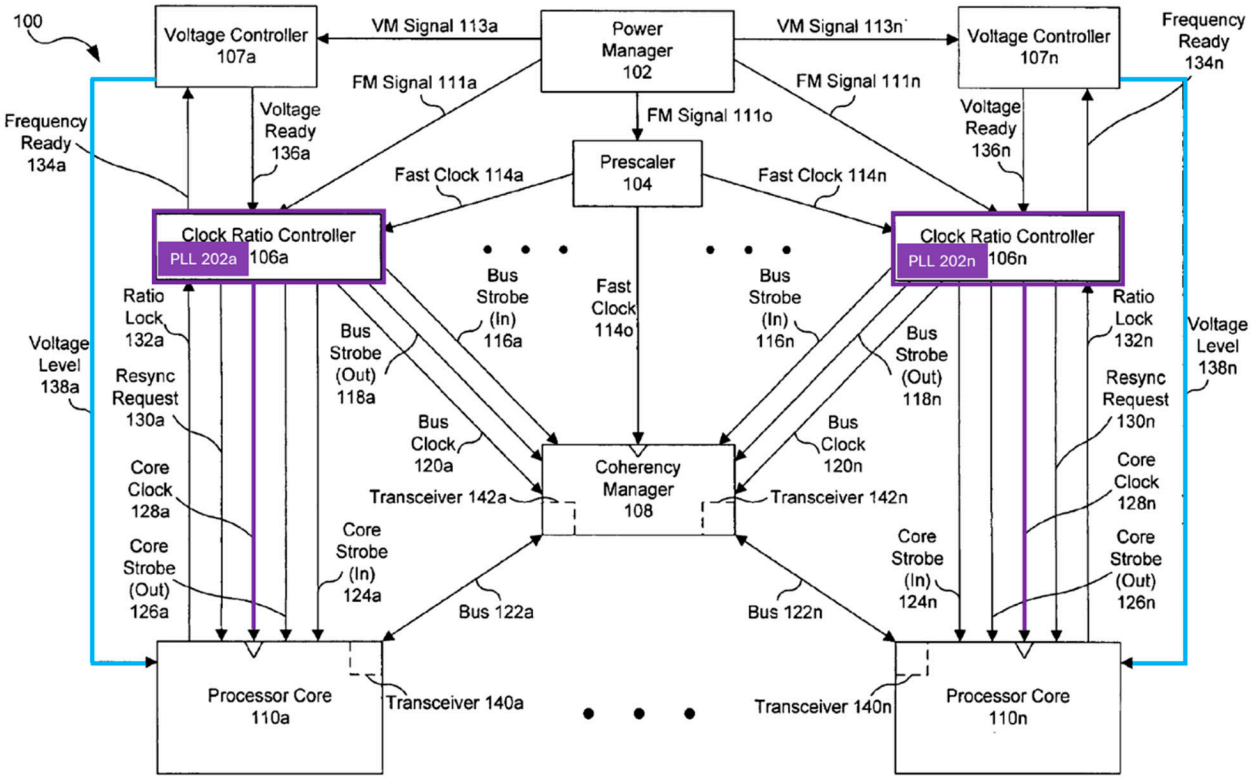
V. The Petition's Ground 1 Fails to Disclose The Claimed First and Second Clock Signals

The Petition fails to identify the key components claimed to enable the management of sets of, rather than individual, cores. Namely, the petition fails to identify a first and second PLL that respectively receive a first and second clock signals that are independent of one another. Instead, the Petition relies on Dr. Baker to manufacture these PLLs and associated clock signals with no explanation for why such would be obvious, inherent, or otherwise disclosed. Likewise, the Petition offers no explanation for why the manufactured clock signals would be independent of the clock signal that was actually disclosed. For any and all of these reasons, Ground 1 fails to demonstrate how any claim is obvious.

A. A First and Second PLLs Are Not Disclosed In the Art

Both challenged independent claims require a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal. *See* Ex. 1001 at Cl. 1, 21. Mediatek's petition proposes a first and second PLL and accompanying first and second clock signals as inputs that are not disclosed in either Knoth or Allarey and not justified as obvious or inherent.

The Petition proposes that the claimed first and second PLLs can be found in either Knoth or Allarey but Knoth fails to disclose two PLLs and the Petition fails to justify any combination with Allarey. For Knoth, the Petition identifies PLL 202_a and PLL 202_n as a component of Clock Ratio Controller 106_a and 106_n. Paper 1 at 22-23.



Id. at 22. However, Knoth never discloses a PLL 202_a or PLL 202_n or any PLL that is a component of a Clock Ratio Controller 106. Both are an ex post invention of Dr. Baker. What Knoth actually discloses is the "clock ratio controller 106 is *coupled to* a phase-lock loop (PLL) 202 and prescaler 104 of digital system 100." Ex. 1005 at

[0041][1]. Indeed, the only figure that depicts any PLL, Figure 2A expressly excludes it from the Clock Ratio Controller 106 via a demarcating dotted line:

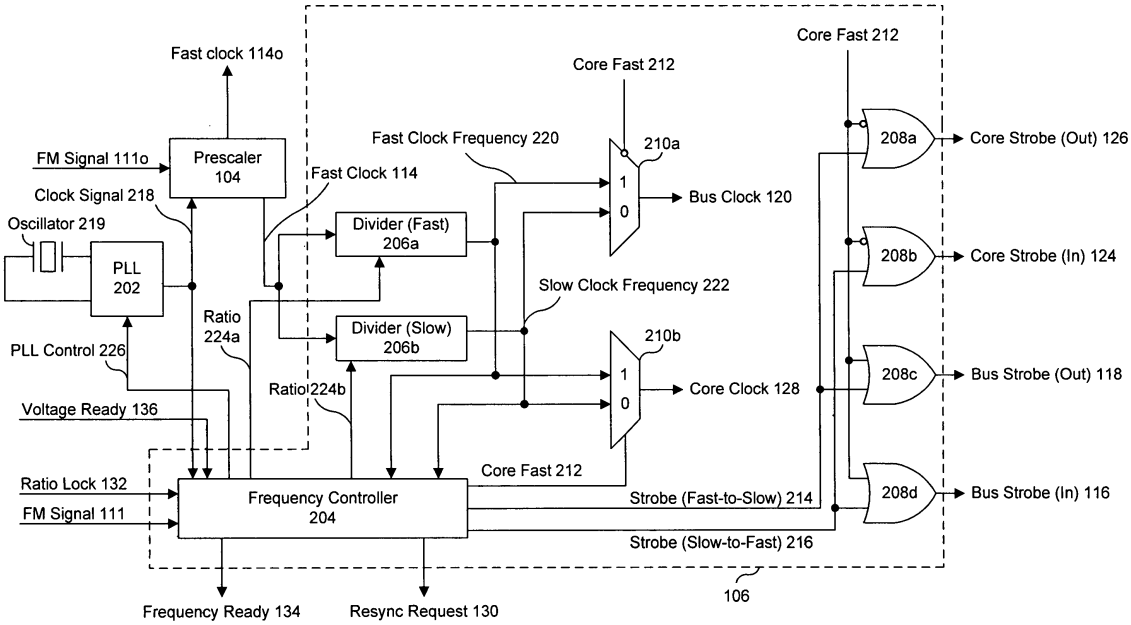


FIG. 2A

Id. at Fig. 2A.

The Petition has no explanation for its creation of an entire series of PLLs. Likewise, looking to Dr. Baker's declaration, there is nothing. At best, Dr. Baker suggests Fig. 2A "shows a representative clock ratio controller 106 that includes PLL 202 and an oscillator 219 [and a]s a result, clock ratio controllers $106_{a\text{-}n}$ each includes a phase locked loop (PLL) 202…" Ex. 1003 at ¶ 111. But, as noted above,

[1] All emphasis is added unless otherwise noted.

PLL 202 is expressly *not* part of the clock ratio controller 106. *See* Ex. 1005 at Fig. 2A and [0041]. Rather, the PLL 202 is treated much more like prescaler 104, a separate part of the digital system 100. *Id*. at [0041] ("clock ratio controller 106 is *coupled to* a phase-lock loop (PLL) 202 and prescaler 104 of digital system 100.") While Knoth discloses "a *plurality* of clock ratio controllers [and] a *plurality* of voltage controllers [and] a *plurality* of processor cores" all designated a–n, it only discloses a single prescaler 104 and a single PLL 202 and never similarly designates them. *Id*. at [0022]; [0041]. Because, as seen in Fig. 1 and discussion throughout Knoth, there is only one prescaler 104, the logical conclusion is that there is only one similarly disposed phase-lock loop 202. But even without making that logical determination, the Board should still reject Dr. Baker's leap as it has no basis or explanation under either obviousness or inherency. *See* 37 CFR § 42.65 ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.").

First, the petition simply makes no obviousness assertion as to this limitation within Knoth.[2] Second, a party suggesting inherency "must show that *the natural result flowing* from the operation as taught would result in the performance of the questioned function." *PersonalWeb Techs., LLC v. Apple, Inc.*, 917 F.3d 1376, 1382

[2] The Petition's reference to Allarey is addressed below.

(Fed. Cir. 2019) (emphasis original; internal citations and quotations omitted). Here neither the Petition nor Dr. Baker offer any such showing. Instead, as shown below in Naffziger single PLL systems were common and workable. *Infra* §VI.B.

The Petition's reliance on Allarey fares little better. While Allarey discloses two PLLs, there is no explanation for why or how Allarey's PLLs could be implemented into the teachings of Knoth, much less that a POSITA would. Indeed, all the Petition provides is a general motivation to combine and that "Allarey also discloses this limitation." Paper 1 at 16–18; 25. The Petition's general motivation to combine Knoth and Allarey has nothing to do with PLLs or why a POSITA would be motivated to use multiple as in Allarey where Knoth teaches only one. Instead, the general motivation to combine contends both references "relate to the same well-known technologies," "are directed to the same field of multi-core processors, address similar problems[,] and propose similar solutions for managing voltage and frequency scaling of multi-core processors." *Id*. at 16. But none of these explanations address what features would be taken from what reference, much less why. The *only* basis the Petition offers for a specific combination of Knoth and Allarey is that "a PHOSITA would have been motivated to modify Knoth to have two sets of cores, rather than two individual cores." *Id*. at 20. But this has no connection to the PLLs

of Allarey. Because there is no explanation for why Allarey's two PLLs would or could be implemented into Knoth, MediaTek has not shown it would be obvious.[3]

Indeed, the control system, including its use and placement of PLLs, seems counter to that taught in Knoth. Knoth suggests a centralized control system where a single "power management unit 102 provide individual frequency management (FM) signals [] to clock ratio controllers [] and individual voltage management (VM) signals." Ex. 1005 at [0025]. These signals initiate frequency and voltage adjustments individually for each core. *Id*. In contrast, Allarey teaches a decentralized system where "[e]ach site includes a phase locked loop (PLL) clock signal generation circuit, … each PLL can change the frequency of the clock signal through a relocking process." Ex. 1006 at 2:50–55. Allarey explains "each site with processor 100 might actively modify the frequency of the cores … [and] may need to modify the frequency of the clock signal being supplied to the cores by PLL 116 and PLL 118." It is unclear then why a system designed around a central power management unit dictating the voltage and frequency provided to the cores would implement the arrangement of a system designed for the cores to alter their own frequency.

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[3] To be clear, Dr. Baker likewise presents no explanation of such a combination in his declaration. Indeed, the discussed sections are largely parroted from Dr. Baker's declaration where he provides nothing more.

As the Petition offers no additional analysis for claim 21 and instead merely cites back to sections of claim 1 discussed above, *see* Paper 1 at 49–51, these criticisms apply equally to claim 1 and 21.

B. First and Second Clock Signals as Input Are Not Disclosed In the Art

The Petition's failure to identify a first and second PLL compounds when the "having a first/second clock signal as input" limitation is considered. Without the claimed second PLL, as in Knoth, there can be no second clock signal as input and Allarey discloses no clock signals as input at all.

For Knoth, the Petition suggests two options for the first and second clock signals, "the timing pulses from oscillator 219_a[4], or alternatively, PLL control signal 226_a," Paper 1 at 24, both fail. While the first option, the timing pulses, is a clock signal, there is only one such signal not a first and second signal as claimed. As with PLL 202, Knoth only discloses a single Oscillator 219 providing only a single timing pulse. Ex. 1005 at [0042]. The single oscillator is depicted as outside of any clock ratio controller 106 (*Id*. at Fig. 2A) and MediaTek identifies no basis for multiplying either an oscillator or a timing pulse to each clock ratio controller. A single signal cannot satisfy either the need for a first and second clock signal.

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[4] Again, there is no 219_a disclosed in Knoth, only a 219 that is separate from any clock ratio controller 106. *See* Ex. 1005 at [0041].

MediaTek's alternative, PLL control signals, are simply not clock signals. Knoth explains "clock ratio controller 106 includes frequency controller 204" and "PLL 202 is controlled by frequency controller 204 using a PLL control signal 226." Ex. 1005 at [0042], [0044]. But neither MediaTek nor Dr. Baker explain why a frequency controller's PLL control signal would be considered a "clock signal" by a POSITA. This is particularly jarring when Knoth itself uses the term "clock signal" with regards to a variety of other signals. *See e.g. id*. at [0042] ("PLL 202 outputs a clock signal 218"); [0043] ("prescaler 104 provides clock signal 218 to clock ratio controller 106 as a fast clock signal 114"). The '339 Patent explains a "clock signal" drives the processor core. Ex. 1001 at 4:4–10. This is the same as Knoth explains its "clock signals" but not PLL control signal. *Compare* Ex. 1005 at [0044] ("Core fast signal 212 is used to indicate whether an associated processor core 110 is to be driven by the output of clock signal divider 206_a or the output of clock signal divider 206_b.") *with* [0061] ("Programmable logic array 250 may also control PLL 202 using PLL control signal 226."). A "clock signal" and a "control signal" are clearly different signals and a PLL control signal does not meet the first and second clock signal limitation. Further, as noted above, Knoth only discloses a single PLL, thus even if a PLL control signal were a "clock signal," Knoth does not disclose "a second PLL having a second clock signal as input."

Allarey does not even disclose inputs to its PLLs and neither Dr. Baker nor MediaTek contend otherwise. *See* Ex. 1003 at ¶ 121 ("Allarey discloses that the first set of cores (cores in site 0) dynamically receives a first supply voltage and a first output clock signal of a first PLL (PLL for site 0)."). Rather, Allarey only teaches "[e]ach PLL is capable of generating a clock signal that the cores located at each respective site can use as a reference clock." Ex. 1006 at 2:52-54. Even if the PLLs of Allarey could or would have been combined with any teaching of Knoth (and MediaTek has not shown such), there would be no first and second clock signals as inputs.

C. The First Clock Signal is Independent from the Second Clock Signals as Input Is Not Disclosed In the Art

All these failures come to a head at the "first clock signal is independent from the second clock signal" limitation. In order to meet this limitation, the Petition relies on only one proposed modification: incorporating a second oscillator. The Petition contends a "PHOSITA would read Knoth to include independent first and second PLLs within clock ratio controllers 106_a and 106_n, respectively, receiving the first and second clock signals (the timing pulses generated by oscillators 219_a and 219_n) that are independent from each other." Paper 1 at 28-29. While the Petition cites Dr. Baker's declaration, he only provides the exact same conclusory language. *See* Ex. 1003 at ¶¶ 131-32.

As explained above, Knoth discloses only a single PLL, a single oscillator, and instance of timing pulses. Neither the Petition nor Dr. Baker's declaration explain why it would be obvious or inherent or would be a PHOSTIA's reading that multiple PLLs, oscillators, or sets of timing pulses could or would be used. And even if the Board accepts that multiple PLLs would be used, that does not disclose multiple independent clock signals as claimed, much less the specific modification relied on in the Petition where the multiple independent clock signals correspond to multiple oscillators.

Indeed, this is the express teaching of Naffziger discussed below. *Infra* §VI.B. Such a device would not have a first and second clock signal, just one clock signal sent to two locations. And even if the Board were to accept multiple oscillators, despite neither Knoth or Allarey teaching such, the Petition offers no explanation for why they would be "independent from each other" as posited by MediaTek. Because the alternative, PLL control signals, are not clock signals, they likewise cannot disclose this limitation.

MediaTek's discussion of Allarey also fails. All MediaTek can contend is that "the first PLL clock signal generation circuit is independent from the second PLL clock generation circuit." Paper 1 at 29. But that is not what is claimed. The claims are not concerned with whether the PLLs, or their associated circuits, are independent, but rather if the input clock signals are. *See* Cl. 1, 21. Even if

MediaTek's conclusion on the independence of Allarey's circuits was supported, it is not, it is entirely irrelevant. Allarey does not disclose "the first clock signal is independent from the second clock signal."

Ground 1 of the Petition fails to demonstrate the claimed first and second PLLs having a respective first and second clock signal as input or the first clock signal is independent from the second clock signal are obvious. First, the Petition does not demonstrate Knoth discloses a first and second PLL or that it would be obvious to incorporate the first and second PLLs from Allarey. Second, Knoth fails to disclose a second clock signal as input and Allarey does not disclose any clock signals as inputs. Last, because neither Knoth nor Allarey disclose a first and second clock signal, neither discloses or renders obvious "the first clock signal is independent from the second clock signal." As such, Ground 1 does not demonstrate any of the challenged claims are obvious much less establish a reasonable likelihood of prevailing at a Final Written Decision.

VI. The Petition's Ground 5 fails for the Same Reason.

Ground 5 suffers the same flaw as Ground 1. There is no disclosure in Naffziger of a second PLL. Instead, Dr. Baker simply invents one. This creation deletes the mode expressly taught by Naffzigger with no explanation offered in the Petition for why Naffzigger's teachings would be disregarding or why a second PLL would be used instead. Likewise, the Petition offers no basis for incorporating any

teaching of Allarey with regard to PLLs or clock signals. As such, just as above, Ground 5 fails to demonstrate the claimed first and second PLLs having a respective first and second clock signal as input or that the first clock signal is independent from the second clock signal are obvious.

A. Ground 5 Discloses Only One PLL

The challenged claims all require a first and second PLL. MediaTek provides only a single theory for Naffziger disclosing two PLLs, that "[a] PHOSITA reading Naffziger would have understood that the multi-core processor 500 includes more than one power control unit 150 each associated with a corresponding core[,]" thus providing a "first power control unit 150A" and a "second power control unit 150B" each contain a PPL. Paper 1 at 69. But Naffziger does not teach multiple power control units instead, it expressly teaches using only a single power control unit.

Naffziger expressly teaches "[p]ower control unit 150 is configured to monitor the power of *both* processor cores 105A and 105B…" Ex. 1010 at [0053] (emphasis added). Indeed, Figure 5 shows only a single power control unit 150 is used and provides "clk_core_1" and "clk_core_2" to Cores 1 and 2:

Second, there is evidence that the Petitioner unduly delayed in filing the Petition, doing so less than four months before the statutory deadline, and the Petitioner offers no explanation for the delay. *See supra* § VII.C.

* * *

Each of the six *Fintiv* factors supports the Board exercising its discretion to deny institution.

VIII. Conclusion

For the reasons set forth above, Patent Owner respectfully requests that the Board deny institution of the Petition. Both Grounds 1 and 5 rely on an unsupported addition to the prior art that a second PLL and second clock signal would exist and that the second clock signal would be independent of the first clock signal. But the Petition never shows these additions would be obvious or inherent.

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CERTIFICATION REGARDING WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner certifies that there are 6,452 words in the paper excluding the portions exempted under 37 C.F.R. §42.24(a)(1).

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on February 5, 2025, by filing this document through the Patent Trial and Appeal Board Cast Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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